WHAT IS CLAIMED IS:

1. A circuit for performing a line loop back test, the circuit comprising:

a receiver that receives an input signal from a receiver communication line;

a deserializer coupled to the receiver that converts high speed serial receiver data derived from an input signal received by the receiver into low speed parallel data;

a low speed parallel loop back data multiplexer coupled to the deserializer that selects either the low speed parallel data from the deserializer or low speed parallel input data;

a serializer coupled to the low speed parallel loop back data multiplexer that converts low speed parallel output data from the low speed parallel loop back data multiplexer into high speed serial transmitter data; and

a transmitter coupled to the serializer that converts the high speed serial transmitter data into an output signal for transmission across a transmitter communication line.

2. A circuit as in claim 1,

wherein the deserializer further produces a low speed clock output signal, further comprising:

a low speed loop back reference clock multiplexer coupled to the deserializer that selects either the low speed clock output signal from the deserializer or a reference clock input signal.

3. A circuit as in claim 2, further comprising:

a clock multiplying unit coupled to the low speed loop back reference clock multiplexer and the serializer that converts a low speed output of the low speed loop back reference clock multiplexer into a high speed clock signal;

wherein the serializer generates the high speed serial transmitter data in synchronization with the high speed clock signal received from the clock multiplying unit.

4. A circuit as in claim 3, further comprising:

a first-in-first-out buffer coupled to the serializer that provides coupling between the serializer and the low speed parallel loop back data multiplexer; and

a low speed loop back clock multiplexer coupled to the first-in-first-out buffer that selects either the low speed clock output signal from the deserializer or a low speed clock input signal; and

a clock divider circuit coupled to the first-in-first-out buffer that converts the high speed clock signal from the clock multiplying unit into a low speed FIFO output clock;

wherein the first-in-first-out buffer receives the low speed parallel output data from the low speed parallel loop back data multiplexer in synchronization with a clock multiplexer output received from the low speed clock multiplexer;

wherein the first-in-first-out buffer transmits low speed parallel FIFO data to the serializer in synchronization with the low speed FIFO output clock received from the clock divider.

5. A circuit as in claim 1, further comprising:

a low speed parallel loop back data buffer that provides coupling between the deserializer and the low speed parallel loop back data multiplexer.

6. A circuit as in claim 2, further comprising:

a low speed loop back clock buffer that provides coupling between the deserializer and the low speed loop back reference clock multiplexer.

7. A circuit as in claim 4, further comprising:

a low speed loop back clock buffer that provides coupling between the deserializer and the low speed loop back reference clock multiplexer, and that provides coupling between the deserializer and the low speed loop back clock multiplexer.

8. A circuit as in claim 1, further comprising:

a clock and data recovery unit that provides coupling between the receiver and the deserializer.

9. A circuit for performing a line loop back test, the circuit comprising:

a serializer that receives a serializer parallel data input signal and that generates a serializer serial data output signal;

a first-in-first-out buffer having a FIFO parallel data input signal and a FIFO parallel data output signal;

a loop back data multiplexer that receives a loop back data multiplexer parallel data input signal and a loop back data multiplexer parallel loop back input signal and that generates a loop back data multiplexer parallel data output signal;

a loop back data buffer that receives a loop back data buffer parallel input signal and that generates a loop back data buffer parallel output signal; and

a deserializer that receives a deserializer serial data input signal and that generates a deserializer parallel data output signal;

wherein the deserializer parallel data output signal is coupled to the loop back data buffer parallel input signal;

wherein the loop back data buffer parallel output signal is coupled to the loop back data multiplexer parallel loop back input signal;

wherein the loop back data multiplexer parallel data output signal is coupled to the FIFO parallel data input signal;

wherein the FIFO parallel data output signal is coupled to the serializer parallel data input signal.

10. A circuit as in claim 9, further comprising:

a clock multiplier unit that receives a clock multiplier unit input signal and that generates a clock multiplier unit output signal;

wherein the serializer further receives a serializer clock input signal;

wherein the clock multiplier unit output signal is coupled to the serializer clock input signal.

11. A circuit as in claim 10, further comprising:

a loop back reference clock multiplexer that receives a loop back reference clock multiplexer reference clock input signal and a loop back reference clock multiplexer loop back input signal and that generates a loop back reference clock multiplexer clock output signal;

wherein the loop back reference clock multiplexer clock output is coupled to the clock multiplier unit input signal.

12. A circuit as in claim 11, further comprising:

a loop back clock buffer that receives a loop back clock buffer input signal and that produces a loop back clock buffer output signal;

wherein the deserializer further generates a deserializer clock output;

wherein the loop back clock buffer output signal is coupled to the loop back reference clock multiplexer loop back input signal;

wherein the deserializer clock output signal is coupled to the loop back clock buffer input signal.

13. A circuit as in claim 12, further comprising:

a loop back clock multiplexer that receives a loop back clock multiplexer clock input signal and a loop back clock multiplexer loop back input signal and that generates a loop back clock multiplexer output signal;

wherein the first-in-first-out buffer further receives a FIFO input clock signal;

wherein the loop back clock multiplexer output signal is coupled to the FIFO input clock signal;

wherein the loop back buffer output signal is coupled to the loop back clock multiplexer loop back input signal.

14. A circuit as in claim 13, further comprising:

a clock divider that receives a clock divider input signal and that generates a clock divider output signal;

wherein the first-in-first-out buffer further receives a FIFO output clock signal;

wherein the clock divider input signal is coupled to the loop back reference clock multiplexer output signal;

wherein the clock divider output signal is coupled to the FIFO output clock signal.

15. A circuit as in claim 13, further comprising:

a loop back control signal;

wherein the loop back reference clock multiplexer further receives a loop back reference clock multiplexer select signal;

wherein the loop back clock multiplexer further receives a loop back clock multiplexer select signal;

wherein the loop back data multiplexer further receives a loop back data multiplexer select signal;

wherein the loop back control signal is coupled to the loop back reference clock multiplexer select signal, the loop back clock multiplexer select signal, and the loop back data multiplexer select signal.

16. A circuit as in claim 15,

wherein when the loop back control signal is asserted,

the loop back reference clock multiplexer is operative to communicate the loop back reference clock multiplexer loop back input signal to the loop back reference clock multiplexer output signal,

the loop back clock multiplexer is operative to communicate the loop back clock multiplexer loop back input signal to the loop back clock multiplexer output signal, and

the loop back data multiplexer is operative to communicate the loop back data multiplexer parallel loop back input signal to the loop back data multiplexer parallel data output signal; and

wherein when the loop back control signal is deasserted,

the loop back reference clock multiplexer is operative to communicate the loop back reference clock multiplexer reference clock input signal to the loop back reference clock multiplexer output signal,

the loop back clock multiplexer is operative to communicate the loop back clock multiplexer clock input signal to the loop back clock multiplexer output signal, and

the loop back data multiplexer is operative to communicate the loop back data multiplexer parallel data input signal to the loop back data multiplexer parallel data output signal.

17. A circuit for performing a line loop back test, the circuit comprising:

a serializer that receives a serializer parallel data input signal and that generates a serializer serial data output signal;

a first-in-first-out buffer having a FIFO parallel data input signal and a FIFO parallel data output signal;

a loop back data multiplexer that receives a loop back data multiplexer parallel data input signal and a loop back data multiplexer parallel loop back input signal and that generates a loop back data multiplexer parallel data output signal; and

a deserializer that receives a deserializer serial data input signal and that generates a deserializer parallel data output signal;

wherein the deserializer parallel data output signal is coupled to the loop back data multiplexer parallel loop back input signal;

wherein the loop back data multiplexer parallel data output signal is coupled to the FIFO parallel data input signal;

wherein the FIFO parallel data output signal is coupled to the serializer parallel data input signal.

18. A circuit as in claim 17, further comprising:

a clock multiplier unit that receives a clock multiplier unit input signal and that generates a clock multiplier unit output signal;

wherein the serializer further receives a serializer clock input signal;

wherein the clock multiplier unit output signal is coupled to the serializer clock input signal.

19. A circuit as in claim 18, further comprising:

a loop back reference clock multiplexer that receives a loop back reference clock multiplexer reference clock input signal and a loop back reference clock multiplexer loop back input signal and that generates a loop back reference clock multiplexer clock output signal;

wherein the loop back reference clock multiplexer clock output is coupled to the clock multiplier unit input signal.

20. A circuit as in claim 19,

wherein the deserializer further generates a deserializer clock output;

wherein the deserializer clock output signal is coupled to the loop back reference clock multiplexer loop back input signal.

21. A circuit as in claim 20, further comprising:

a loop back clock multiplexer that receives a loop back clock multiplexer clock input signal and a loop back clock multiplexer loop back input signal and that generates a loop back clock multiplexer output signal;

wherein the first-in-first-out buffer further receives a FIFO input clock signal;

wherein the loop back clock multiplexer output signal is coupled to the FIFO input clock signal;

wherein the deserializer clock output signal is coupled to the loop back clock multiplexer loop back input signal.

22. A circuit as in claim 21, further comprising:

a clock divider that receives a clock divider input signal and that generates a clock divider output signal;

wherein the first-in-first-out buffer further receives a FIFO output clock signal;

wherein the clock divider input signal is coupled to the loop back reference clock multiplexer output signal;

wherein the clock divider output signal is coupled to the FIFO output clock signal.

23. A circuit as in claim 21, further comprising:

a loop back control signal;

wherein the loop back reference clock multiplexer further receives a loop back reference clock multiplexer select signal;

wherein the loop back clock multiplexer further receives a loop back clock multiplexer select signal;

wherein the loop back data multiplexer further receives a loop back data multiplexer select signal;

wherein the loop back control signal is coupled to the loop back reference clock multiplexer select signal, the loop back clock multiplexer select signal, and the loop back data multiplexer select signal.

24. A circuit as in claim 23,

wherein when the loop back control signal is asserted,

the loop back reference clock multiplexer is operative to communicate the loop back reference clock multiplexer loop back input signal to the loop back reference clock multiplexer output signal,

the loop back clock multiplexer is operative to communicate the loop back clock multiplexer loop back input signal to the loop back clock multiplexer output signal, and

the loop back data multiplexer is operative to communicate the loop back data multiplexer parallel loop back input signal to the loop back data multiplexer parallel data output signal; and

wherein when the loop back control signal is deasserted,

the loop back reference clock multiplexer is operative to communicate the loop back reference clock multiplexer reference clock input signal to the loop back reference clock multiplexer output signal,

the loop back clock multiplexer is operative to communicate the loop back clock multiplexer clock input signal to the loop back clock multiplexer output signal, and

the loop back data multiplexer is operative to communicate the loop back data multiplexer parallel data input signal to the loop back data multiplexer parallel data output signal.

25. A circuit for performing a line loop back test, the circuit comprising:

a serializer that receives a serializer parallel data input signal and that generates a serializer serial data output signal;

a loop back data multiplexer that receives a loop back data multiplexer parallel data input signal and a loop back data multiplexer parallel loop back input signal and that generates a loop back data multiplexer parallel data output signal;

a loop back data buffer having a loop back data buffer parallel input signal and a loop back data buffer parallel output signal; and

a deserializer that receives a deserializer serial data input signal and that generates a deserializer parallel data output signal;

wherein the deserializer parallel data output signal is coupled to the loop back data buffer parallel input signal;

wherein the loop back data buffer parallel output signal is coupled to the loop back data multiplexer parallel loop back input signal;

wherein the loop back data multiplexer parallel data output signal is coupled to the serializer parallel data input signal.

26. A circuit as in claim 25, further comprising:

a clock multiplier unit that receives a clock multiplier unit input signal and that generates a clock multiplier unit output signal;

wherein the serializer further receives a serializer clock input signal;

wherein the clock multiplier unit output signal is coupled to the serializer clock input signal.

27. A circuit as in claim 26, further comprising:

a loop back reference clock multiplexer that receives a loop back reference clock multiplexer reference clock input signal and a loop back reference clock multiplexer loop back input signal and that generates a loop back reference clock multiplexer clock output signal;

wherein the loop back reference clock multiplexer clock output is coupled to the clock multiplier unit input signal.

28. A circuit as in claim 27, further comprising:

a loop back clock buffer that receives a loop back clock buffer input signal and that produces a loop back clock buffer output signal;

wherein the deserializer further generates a deserializer clock output;

wherein the loop back clock buffer output signal is coupled to the loop back reference clock multiplexer loop back input signal;

wherein the deserializer clock output signal is coupled to the loop back clock buffer input signal.

29. A circuit as in claim 28, further comprising:

a loop back control signal;

wherein the loop back reference clock multiplexer further receives a loop back reference clock multiplexer select signal;

wherein the loop back data multiplexer further receives a loop back data multiplexer select signal;

wherein the loop back control signal is coupled to the loop back reference clock multiplexer select signal and the loop back data multiplexer select signal.

30. A circuit as in claim 29,

wherein when the loop back control signal is asserted,

the loop back reference clock multiplexer is operative to communicate the loop back reference clock multiplexer loop back input signal to the loop back reference clock multiplexer output signal, and

the loop back data multiplexer is operative to communicate the loop back data multiplexer parallel loop back input signal to the loop back data multiplexer parallel data output signal; and

wherein when the loop back control signal is deasserted,

the loop back reference clock multiplexer is operative to communicate the loop back reference clock multiplexer reference clock input signal to the loop back reference clock multiplexer output signal, and

the loop back data multiplexer is operative to communicate the loop back data multiplexer parallel data input signal to the loop back data multiplexer parallel data output signal.

31. A circuit for performing a line loop back test, the circuit comprising:

a serializer that receives a serializer parallel data input signal and that generates a serializer serial data output signal;

a loop back data multiplexer that receives a loop back data multiplexer parallel data input signal and a loop back data multiplexer parallel loop back input signal and that generates a loop back data multiplexer parallel data output signal; and

a deserializer that receives a deserializer serial data input signal and that generates a deserializer parallel data output signal;

wherein the deserializer parallel data output signal is coupled to the loop back data multiplexer parallel loop back input signal;

wherein the loop back data multiplexer parallel data output signal is coupled to the serializer parallel data input signal.

32. A circuit as in claim 31 further comprising:

a clock multiplier unit that receives a clock multiplier unit input signal and that generates a clock multiplier unit output signal;

wherein the serializer further receives a serializer clock input signal;

wherein the clock multiplier unit output signal is coupled to the serializer clock input signal.

33. A circuit as in claim 32, further comprising:

a loop back reference clock multiplexer that receives a loop back reference clock multiplexer reference clock input signal and a loop back reference clock multiplexer loop back input signal and that generates a loop back reference clock multiplexer clock output signal;

wherein the loop back reference clock multiplexer clock output is coupled to the clock multiplier unit input signal.

34. A circuit as in claim 33,

wherein the deserializer further generates a deserializer clock output;

wherein the loop back reference clock multiplexer loop back input signal is coupled to the deserializer clock output signal.

35. A circuit as in claim 34, further comprising:

a loop back control signal;

wherein the loop back reference clock multiplexer further receives a loop back reference clock multiplexer select signal;

wherein the loop back data multiplexer further receives a loop back data multiplexer select signal;

wherein the loop back control signal is coupled to the loop back reference clock multiplexer select signal and the loop back data multiplexer select signal.

36. A circuit as in claim 35,

wherein when the loop back control signal is asserted,

the loop back reference clock multiplexer is operative to communicate the loop back reference clock multiplexer loop back input signal to the loop back reference clock multiplexer output signal, and

the loop back data multiplexer is operative to communicate the loop back data multiplexer parallel loop back input signal to the loop back data multiplexer parallel data output signal; and

wherein when the loop back control signal is deasserted,

the loop back reference clock multiplexer is operative to communicate the loop back reference clock multiplexer reference clock input signal to the loop back reference clock multiplexer output signal, and

the loop back data multiplexer is operative to communicate the loop back data multiplexer parallel data input signal to the loop back data multiplexer parallel data output signal.

37. A method of performing a line loop back test, the method comprising the steps of:

(a) receiving an input signal from a receiver communication line;

(b) converting high speed serial receiver data derived from an input signal into low speed parallel data;

(c) selecting by a low speed parallel loop back data multiplexer either the low speed parallel data or low speed parallel input data as low speed parallel output data;

(d) converting the low speed parallel output data into high speed serial transmitter data; and

(e) converting the high speed serial transmitter data into an output signal for transmission across a transmitter communication line.

38. A method as in claim 37,

wherein step (b) further comprises the step of:

(f) producing a low speed clock output signal;

the method further comprising the step of:

(g) selecting by a low speed loop back reference clock multiplexer either the low speed clock output signal or a reference clock input signal.

39. A method as in claim 38, further comprising the step of:

(h) converting a low speed output of step (g) into a high speed clock signal;

wherein step (d) comprises the step of:

(i) generating the high speed serial transmitter data in synchronization with the high speed clock signal.

40. A method as in claim 39,

wherein a first-in-first-out buffer provides coupling between a serializer that performs step (d) and a low speed parallel loop back data multiplexer that performs step (c);

the method further comprising the step of:

selecting by a low speed loop back clock multiplexer coupled to the first-in-first-out buffer either the low speed clock output signal or a low speed clock input signal;

converting by a clock divider circuit coupled to the first-in-first-out buffer the high speed clock signal into a low speed FIFO output clock;

receiving by the first-in-first-out buffer the low speed parallel output data from a low speed parallel loop back data multiplexer in synchronization with a clock multiplexer output received from the low speed clock multiplexer; and

transmitting by the first-in-first-out buffer low speed parallel FIFO data to the serializer in synchronization with the low speed FIFO output clock received from the clock divider.

41. A method as in claim 37,

wherein a low speed parallel loop back data buffer provides coupling between a deserializer that performs step (b) and a low speed parallel loop back data multiplexer that performs step (c).

42. A method as in claim 38,

wherein a low speed loop back clock buffer provides coupling between a deserializer that performs step (f) and a low speed loop back reference clock multiplexer that performs step (g).

43. A method as in claim 40,

wherein a low speed loop back clock buffer provides coupling between the deserializer that performs step (f) and a low speed loop back reference clock multiplexer, and that provides coupling between the deserializer that performs step (f) and the low speed loop back clock multiplexer.

44. A method as in claim 37,

wherein a clock and data recovery unit provides coupling between a receiver that performs step (a) and a deserializer that performs step (b).